DARK CURRENT CHARACTERIZATION IN CCD's

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Introduction.

To investigate the nature of dark current in CCD's many test structures have been made. All of them have the disadvantage that they do not represent the sensor close enough to extract the relevant dark current parameters. To avoid this the sensor itself has been used as a test structure. DC measurements of dark current versus gate voltage as mentioned by McGrath [1] have been taken. With an additional conductive glue layer on the image section we have determined the influence of the window in the polysilicon gates (figure 1) with respect to the dark current. By pulsing the gates the bulk and interface contribution has been found.

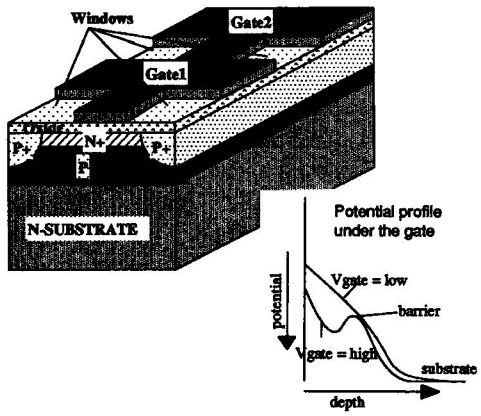

Figure 1 *Image pixel with potential profile.*

Device description and measuring methods.

A frame transfer bulk CCD sensor has been used for the measurements. The device has an image and a storage section, a horizontal register and an output stage.
Each image cell has a n-p-n structure with vertical antiblooming and p+ channel stops to drain holes (figure 1). The polysilicon gates have windows to obtain better light sensitivity. At low gate potentials the generated charge goes to the substrate. At high gate potentials the charge will be kept under the gate because of the potential barrier (figure 1 potential profile).
Two type of measurements have been performed: AC and DC measurements. In the AC measurement the generated charge is transported to the output with a 4 phase transport scheme. The gates are pulsed from -5 to 10 volts. All other potentials are DC. With the DC measurements the gates are all on the same DC potential. The generated charge reaches the output by diffusion.

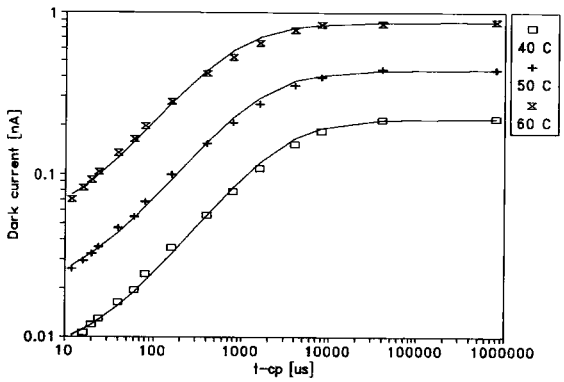

Figure 2 *Pulsed measurements for 3 different temperatures (40,50,60 °C).*

Bulk and interface contribution.

To determine the bulk and the interface contribution we have performed AC measurements on the storage section. When the gates are negative an inversion layer is created at the interface and the interface dark current is suppressed. After removing the layer it will take time to fill the traps, after which they will generate dark current again.
Dark current measurements have been performed as a function of the period time t_{cp}. The results are plotted in figure 2 for three different temperatures. When t_{cp} is large the sum of the bulk and the interface dark current is measured. With a short t_{cp} the interface contribution will be eliminated and only the bulk contribution is measured. Diffusion and trapping of holes limits the frequency so that it was not possible to measure only the bulk contribution. Therefore a model as presented by [3] has been used to fit the data and to extract the bulk and interface contributions separately. The calculated data are shown as lines in figure 2. The fitted parameters are shown in table I. It is clear that the bulk dark current is 20 to 30 times less than the surface dark current.
The values for D_{it} and σ agree with values found in the literature [3].

Table I Fitted parameters of the dark current of interface and bulk.

	40°C	51°C	60°C
$I_{interface}$ (pA)	379	767	1546
I_{bulk} (pA)	12	27	68
D_{it} ($eV^{-1}cm^{-2}$)	$3.7*10^{8}$		
$\sigma_{interface}$ (cm^{2})	$1*10^{-15}$		

Channel and channel stops contribution.

When the dark current in the storage section has to be observed the image gates must be at a low potential. The dark current is measured as a function of gate potential. The result of the storage dark current measurements is shown in figure 3 (measurement curve). At a gate potential of about 3 V the channel has formed and the electrons will no longer go to the substrate. Dark current can then be measured at the output stage. At higher voltages, to 8 volts, the dark current

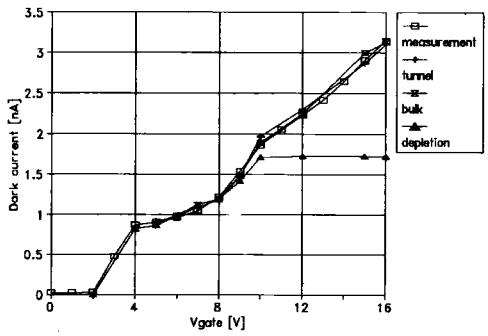

Figure 3 *Storage dark current contribution as a function of gate potential: measurements and calculations with 3 different models.*

increases a little. This is because of the increase of depletion layer near the channel stops. For a gate potentials between 8 and 10 volt the interface of the channel stop is also depleted. At gate voltages of 10 volt and higher the whole interface is depleted. We have simulated the dark current with a 3-D off state simulation package. With the standard SRH recombination model for the interface the dark current is constant for voltages higher than 10 volts (depletion curve). However the measured dark current increases rapidly with gate potential. This can be modelled with a tunnel model (curve tunnel) as presented by Hurkx [2] or by a bulk states model (curve bulk).
From the DC measurements from the storage it is clear that the dark current generated under the gates is about the same as the dark current generated above the channel stop with a gate voltage of 10 volt (default camera voltage). To fit the data we must assume that the channel stop interface has two times more generation states than the interface above the channel. This is reasonable because of the high doping level with high implantation energy in the channel stop.
The simulations with the tunnel model and with the bulk model both fit the data. From gated diode measurements (p-well in n-substrate), however, whenthe interface above the channel stop is inverted the dark current decreases to very low values. A bulk model can not explain this.

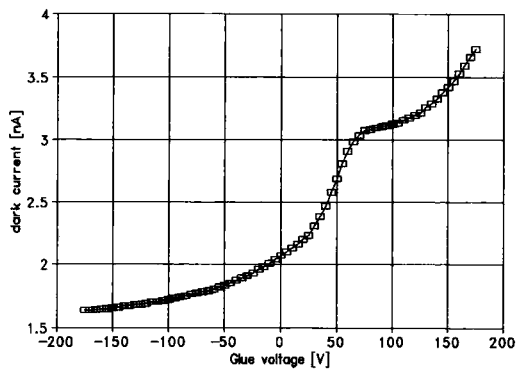

Figure 4 *Image dark current as a function of glue potential.*

Window and channel contribution in the image.

For measuring the dark current in the image section the storage gates must be at a high potential. The image dark current is the measured current minus the storage dark current. In order to determine the dark current contribution from the windows in the image gates a conductive glue layer is put on the image section and is connected to a power supply. In figure 4 the dark

current is plotted as a function of the glue potential. The glue potential must be higher than normal gates because of the large distance of the glue to the interface. The gate potential is 10 volt. The dark current of the image without the glue and with a gate potential of 10 volt is 2.1 nA. This corresponds to 0 volts on the glue. We can see from figure 4 that the dark current from the windows is very sensitive to the interface potential. Therefore oxide charge and the dope profile can have a great influence on the dark current.
At negative glue potentials the window will be accumulated with holes and only the contribution from the interface under the gates is measured. At a glue potential of about 25 volt the window is depleted. For higher potentials the channel stops will be depleted and the dark current will increase because of larger fields or more bulk states. The dark current from the interface under the gates is 1.7 nA. The window contribution measured under normal circumstances is 2.1 - 1.7 = 0.4 nA. The window contribution is much smaller than the gate contribution because the window interface is only partly depleted in the normal situation with no glue.

Conclusions.

- Bulk dark current is about 20 times smaller then interface dark current.
- The tunnel and the bulk model can fit the measured data from the storage dark current.
- The interface state density above the channel stop is about two times higher than under the gate.
- Contributions from the image and storage area are about the same.
- The window contribution is about 20 % of the total image dark current, but is strongly dependent on the interface potential.
- A complete characterization of dark current in these CCD's needs only a few DC voltages, some pulse generators and a DC current meter

references.

[1] R.D. McGrath, ESSDERC conference september 1992, page 627.
[2] G.A.M Hurkx, IEEE Transactions on electron devices vol. 39, No. 2, February 1992
[3] Barry E. Burke, IEEE Transactions on electron devices vol. 38, No. 2, February 1991.